conducted, using an abrasive slurry, to remove the Ta or TaN barrier layer. ~~A suitable buffing technique is disclosed in co-pending U.S. patent application Serial No. 09/401,643, filed on September 22, 1999, the entire disclosure of which is incorporated by reference herein.~~ The surface of the silicon oxide interlayer dielectric is also buffed to reduce or eliminate scratching and defects. The polishing pads are mounted on rotating platens. Multi-station CMP systems are commercially available, such as the Mirra® polisher, available from Applied Materials, Inc., Santa Clara, California.

Please replace the paragraph at page 14, line 15, to page 15, line 2, with the following paragraph:

For example, in an interconnection system comprising a silicon dioxide interlayer dielectric and TaN barrier layer, the chemical agent can comprise about 1 to about 10 wt.% of an oxidizer, e.g., about 6 wt.%, such as hydrogen peroxide, about 0.05 to about 0.20 wt.% of an inhibitor, e.g., about 0.15 wt.%, such as 5-methyl benzotriazole, about 1.0 to about 5.0 wt.% e.g., about 3 wt.%, of a chelating agent, such as iminodiaetic acid, and about 3.0 to about 15.0 wt.%, e.g., about 9.0 wt.%, of another chelating agent, such as ammonium hydrogen phosphate, the balance deionized water. The pressure is typically about 3 psi. The concentration of the inhibitor can be strategically adjusted throughout the polishing steps of the present invention to control the static etching rate. For example, the static etching rate can be decreased by increasing the amount of inhibitor, thereby reducing chemical complexing of Cu by chelating components of the chemical agent.

Please replace the paragraph at page 16, lines 7-29, with the following paragraph:

The wafer surface is then buffed, in a conventional manner ~~or as disclosed in a pending U.S. patent application Serial No. 09/401,643, filed on September 22, 1999, with abrasive, to remove the Ta or TaN barrier layer, under conditions such that there is no reversed selectivity among the silicon oxide interlayer dielectric, barrier layer and Cu~~. Embodiments of the present invention comprise further refinements to minimize dishing. It was found that dishing can be controlled during CMP steps (a) and (b) by controlling one or more processing features or parameters. For example, embodiments of the present